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Accurate Dielectric Capacitance Determination from Metal-Insulator-Semiconductor Devices Having Bias and Frequency Dependent Conductance Due To Leakage Current

Ravi Kumar Chanana
Department of Electrical and Electronics Engineering, Galgotia's College of Engineering and Technology, Affiliated to Uttar Pradesh Technical University, Lucknow, 1, Institutional Area, Knowledge Park-II, Greater Noida-201306, India.

Abstract: *A model for MIS device in accumulation is proposed which includes a bias and frequency dependent conductance in parallel with the insulator capacitance due to the leakage current. The model is validated by experimental results on MOS structures fabricated on n<100>Si having about 9 nm dry thermal oxide. The real and imaginary impedance versus frequency plots of such MOS device having large conductance can be used to determine accurately the oxide capacitance and consequently the oxide thickness without the use of ellipsometer. Greatly reduced MIS dot area can assist in avoiding frequency dispersion in accumulation capacitance, particularly at small-signal frequency of 1 MHz which is commonly used for generating high frequency C-V plots.*

Keywords: *Metal-Insulator-Semiconductor, Impedance, Conductance*

I. Introduction

As the Ultra Large Scale Integration (ULSI) CMOS technology progresses, the device dimensions will shrink further with channel lengths below 50 nm and the gate oxide thickness in the 1.0-2.5 nm range. For such thin oxides, the tunneling current is high resulting in the existence of significant conductance in parallel with the oxide capacitance in accumulation. This conductance causes frequency dispersion of Metal-Insulator-Semiconductor (MIS) device accumulation capacitance, particularly for large area MIS dots. Also, ultrathin thermal SiO_2 in the 1-2 nm range has been studied earlier, but the frequency dispersion discussed was corrected by making measurements at two different frequencies [1]. The author in this paper presents a MIS model that explains frequency dispersion of accumulation capacitance in a oxide insulator having leakage current of 26 μA at 0.5 V accumulation bias. A method is given to obtain the static oxide capacitance and oxide thickness without the ellipsometric measurements for oxide insulator thickness determination along with the determination of series resistance and the oxide conductance at a particular accumulation bias and at only one frequency point. A similar model has been proposed earlier [2] but the method and measuring equipment used to obtain the parameters are different. Some other applications of MIS devices have been mentioned in the introduction of author's earlier article [3]. More recently, numerical simulation of a passivated emitter solar cell is performed [4] and an MIS photoanode finds use in artificial photosynthesis experiment of water-splitting where the thin tunnel oxide protects the Si from corrosion due to evolving O_2 at the anode [5]. MIS devices are also used in internal photoemission experiments to determine band offsets of MIS interfaces [6] in which the applied field across the insulator can be corrected by the flatband voltage [7].

II. Experimental

The MIS sample was prepared on n<100>Si polished wafer having 1-6 Ω-cm resistivity and 50 mm diameter. This wafer was oxidized in 100% dry O_2 ambient at 850^{o}C for 40min in a standard atmosphere furnace after the wafer had undergone cleaning in a hot mixture of 2:1 H_2SO_4:H_2O_2 followed by a 30s dip in 1% HF solution and rinse in DI water and spin dry. Front and back Al metallization followed by 7min anneal in N_2 ambient at 450^{o}C completed the fabrication of the MOS sample having a dot area of 0.6 mm^2 and the oxide thickness of about 9 nm. The small-signal capacitance and conductance versus bias plot at different frequencies and the parallel capacitance and real and imaginary impedance versus frequency plots at a given accumulation bias of 0.5 V were obtained on the HP4194A impedance analyzer connected to the HP7090A measurement plotting system. These plots are presented in figures 1, 2 and 4.

III. Results and Discussion

3.1 MIS Device Model in Accumulation

Figure 1 is a small-signal (10mV rms) capacitance and conductance versus bias plot at four different frequencies of 5, 100, 500 and 1000 KHz, clearly demonstrating the dispersion in the accumulation capacitance. At a given bias, the accumulation capacitance is decreasing with increasing frequency and the conductance is increasing with increasing frequency. This is also shown in Fig. 2 by the parallel capacitance and conductance versus frequency plot at a given bias of 0.5V across a MOS capacitor. The frequency dispersion in accumulation capacitance is a combination of extrinsic and intrinsic effects in the current-voltage characteristics of the MOS capacitor having thermal SiO_2 as the dielectric [8]. The review article of reference [8] separates the extrinsic and intrinsic effects of frequency dispersion in the current-voltage characteristics of the MOS capacitor and also reviews the dielectric relaxation and resonance models pertaining to the intrinsic effects at high frequencies. The real part of the complex permitivity is due to dielectric relaxation having the nature of permitivity as a function of frequency representing a capacitor, and the imaginary part of the complex permitivity which is due to dielectric resonance is of the nature of σ/ω, where σ is the conductivity of the SiO_2 dielectric and ω is the frequency of the applied electric field. This conductivity can be modeled as a resistance representing energy loss due to dielectric resonance. The extrinsic effects reviewed are the following: surface roughness, polysilicon depletion, quantum confinement, parasitic effects such as series resistance, back contact imperfections and cable connections, oxide tunneling leakage current, and interfacial lossy layer of SiO_x. All the extrinsic effects except leakage are eliminated in the MOS sample of the present study. The MOS sample of the present study is in accumulation, so there is no capacitance due to interface states and depletion, the back contact is a very large area of 19.6 cm^2, the gate metal is Al eliminating polysilicon depletion, and the oxide thickness is about 9 nm having leakage of 26 µA at 0.5 V accumulation bias. Therefore, the frequency dispersion observed and presented in figures 1, 2, and 4 is due to a leaky oxide. Fig. 3a represents the simplified model of the MOS capacitor test structure in accumulation [9] and Fig. 3b is the modified model that the author proposes, in which a frequency and bias dependent conductance $G_{ox}(V, \omega)$ is connected in parallel to the oxide capacitance and is causing the dispersion in capacitance shown in Fig. 1 and Fig. 2. $R_s$is the series resistance which is known to exist due to various sources [9].

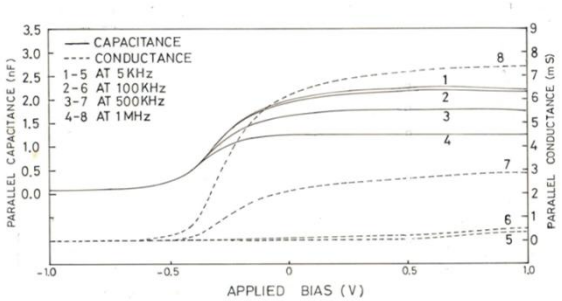

Fig.1 Typical High-frequency C-V and G-V plots at four different small-signal frequencies on n<100>Si MOS device.

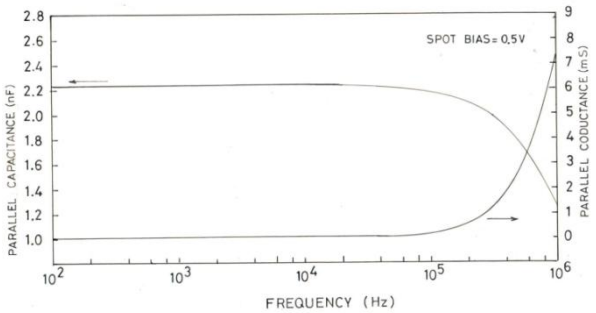

Fig.2 Typical parallel capacitance and conductance versus small-signal frequency plots at a accumulation bias of 0.5 V across n<100>Si MOS device.

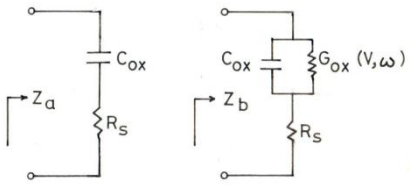

Fig.3 MIS model in accumulation---a) simplified, on the left, and b) proposed, having significant conductance, on the right.

The impedance of Fig. 3b is given by:

$$Z_b = \frac{1}{G_{ox} + j\omega C_{ox}} + R_s \tag{1}$$

For very small G_{ox}, this impedance reduces to that of Fig. 3a and expressed as:

$$Z_a = \frac{1}{j\omega C_{ox}} + R_s \tag{2}$$

Rationalizing Z_b and separating the real and imaginary parts, we get:

$$Z_b = \left[R_s + \frac{G_{ox}}{G_{ox}^2 + \omega^2 C_{ox}^2} \right] - j\left[\frac{\omega C_{ox}}{G_{ox}^2 + \omega^2 C_{ox}^2} \right] \tag{3}$$

The real part of Z_b in equation 3 can be re-written as:

$$\mathrm{Re}(Z_b) = \frac{\frac{1}{G_{ox}}}{1 + \frac{\omega^2}{\omega_{ox}^2}} + R_s \tag{4}$$

where, $\omega_{ox} = \frac{G_{ox}}{C_{ox}}$.

Now, for $\omega << \omega_{ox}$, $\mathrm{Re}(Z_b) = R_s + \frac{1}{G_{ox}}$, and

For $\omega >> \omega_{ox}$, $\mathrm{Re}(Z_b) = R_s + \frac{\omega_{ox}^2}{\omega^2 G_{ox}}$.

This relation is exhibited by the plot of Re (Z_b) versus ω in Fig. 4 validating the model. The characteristic frequency ω_{ox} is dependent on the accumulation bias and is thus a particular value at a given accumulation bias. The imaginary part of Z_b in equation 3 can be re-written as:

$$\mathrm{Im}(Z_b) = -\frac{\omega C_{ox}}{G_{ox}^2 + \omega^2 C_{ox}^2} \tag{5}$$

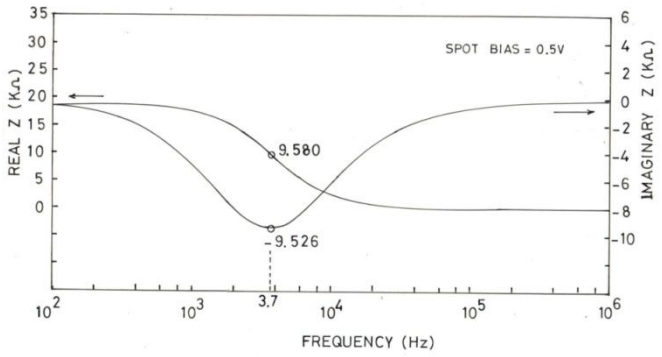

Fig.4 Typical real and imaginary impedance versus small-signal frequency plots at 0.5 V accumulation bias across the MOS device.

Here, for large G_{ox} and small ω, -Im (Z_b) is proportional to ω and for large G_{ox} and large ω, -Im (Z_b) is proportional to $1/\omega$. This relation is also exhibited in the plot of Im (Z_b) versus ω in Fig. 4, further validating the model.

1.2 Determination of C_{ox}, G_{ox} and R_s

As can be observed in Fig. 4, the plot of Im (Z_b) versus frequency has a minimum at frequency ω_{ox}, which can be used to determine G_{ox} and C_{ox}. Differentiating equation 5 with respect to frequency and equating it to zero gives the condition for minimum Im (Z_b) as:

$$G_{ox} = \omega_{ox} C_{ox}.$$

Substituting this relation in equation 5 yields:

$$\min \mathrm{Im}(Z_b) = -\frac{1}{2\omega_{ox}C_{ox}} = -\frac{1}{2G_{ox}} \qquad (6)$$

From the known values of ω_{ox} at minimum Im (Z_b), C_{ox} and G_{ox} can be determined.

Using the value of minimum Im (Z_b) 0f -9.526 KΩ at ω_{ox}= 3.7 KHz indicated in Fig. 4 for the n-MOS sample used, gives C_{ox} of 2248 pF which is an accurate static capacitance of the thin thermal oxide of 9.2 nm having an ε_r of 3.9 and a dot area of 0.6 mm^2. Equation 6 can also be used to determine G_{ox} at 0.5V bias to be 0.0525 mS. Also, as shown in Fig. 4, using the value of Re (Z_b) 0f 9.580 KΩ at the same frequency of 3.7 KHz where Im (Z_b) occurs, equation 4 yields the value of R_s as 54 Ω. It must be noted at this point that G_{ox} is a function of both bias and frequency as clearly demonstrated in Fig. 1 and Fig. 2. It can be observed that at low frequencies of a few KHz, the resistance of the bulk oxide dominates the conductance and at higher RF frequencies the capacitance dominates the conductance. The minimum in Im (Z_b) occurs at a low value of 3.7 KHz, as shown in Fig. 4. The use of the above method of determining C_{ox}, G_{ox} and R_s is valid and accurate. A higher value of G_{ox}, say at a larger accumulation bias, will shift the valley of Im (Z_b) versus frequency plot to the right and at a lower G_{ox} will shift it to the left. In equation 1, if G_{ox} is much less than ωC_{ox}, then G_{ox} can be neglected and the equation reduces to equation 2 which expresses the impedance of a non-leaky MOS in accumulation [9]. Hence,

$$G_{ox} << \omega C_{ox} \qquad (7)$$

is the condition to be fulfilled for obtaining no dispersion in accumulation capacitance. Also, if the MOS dot area is reduced, C_{ox} and G_{ox} will reduce, increasing the impedance and consequently the onset of frequency dispersion in accumulation capacitance will occur at higher frequency. Therefore, for C-V and I-V analysis of thin dielectric having large conductance at accumulation biases and at high small-signal frequencies such as 1 MHz, the dot area should be greatly reduced to avoid frequency dispersion in accumulation capacitance, which would then yield correct static capacitance of the insulator. The advantages of using this method of C_{ox} determination as compared to the method of Yang and Hu [1] or Yao et al [2] are the following:

1) The measurements of real and imaginary impedances are required at only one frequency.
2) The leakage current is believed to be due to defects, such as oxygen vacancies in SiO_2 [10, 11] where the current takes the form of hopping conduction through the bulk at very low electric fields such as (0.5/0.92) MV/cm in the present study [12]. After correcting for leakage current, it can be observed from Yang and Hu's paper [1], that the capacitance in accumulation is constant for all biases in accumulation. Therefore determination of accumulation capacitance at one bias point in accumulation is sufficient.
3) The final C-V curve can be obtained after obtaining C_{ox} through a simple software program.
4) Al metal gate is used in the present study. For oxides of thickness less than 10 nm, polysilicon depletion potential [13] can cause error in C_{ox} measurements. Yang and Hu have used n^+ polysilicon contact but do not mention any errors due to polysilicon depletion. It could be that the potential due to polysilicon depletion is negligibly small due to the polysilicon being very heavily doped such as $10^{20}/cm^3$ with Phosphorus or Arsenic atoms, and/or polysilicon depletion potential has large values only at high electric fields. This can be observed in figure 3 of the study of Depas et al [14], where the polysilicon depletion at higher voltages adds to the oxide thickness and reduces the accumulation capacitance.

At this point, the author wishes to clarify a confusion about the sign of polysilicon depletion potential, say V_{poly} in an n-channel MOSFET with positive voltage at the n^+ polysilicon gate. The gate voltage V_G is given by:

$$V_G = V_{fb} + V_{ox} + V_s \qquad (8)$$

If V_G in equation (8) is a measured quantity, then it is corrected by subtracting V_{poly} [14-16] which can be calculated [13]. V_G is then given as:

$$V_G = V_{fb} + V_{ox} + V_s - V_{poly} \qquad (9)$$

If V_G in equation (8) is a corrected value, then V_{poly} is added to make it as measured [17]. It is then given as:

$$V_G = V_{fb} + V_{ox} + V_s + V_{poly} \qquad (10)$$

IV. Conclusion

It is inferred from the study that frequency dispersion in accumulation capacitance of MOS devices with thin and ultrathin oxide occurs due to high leakage current and can be modeled as a bias and frequency dependent conductance in parallel with the oxide capacitance. This dispersion can be avoided by reducing the MOS dot area so as to increase the oxide resistance. Also, accurate determination of C_{ox}, G_{ox} and R_s can still be made from the real and imaginary impedance versus frequency plots at a given accumulation bias without the use of ellipsometer. Consequently, the oxide thickness can be determined accurately. The advantages of this method of C_{ox} determination are mentioned above in discussion. Polysilicon depletion potential in MOS device having heavily doped polysilicon gate contact can be a source of error in the determination of ultrathin oxide thickness. It can be eliminated by having low accumulation bias such as 0.5V in the present study. The MOS sample of the present study however has Al gate thereby completely eliminating polysilicon depletion.

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